

**REMARKS:**

**Claim Rejections Under 35 USC 102:**

Claims 1-9 and 22 were rejected under 35 USC 103(a) as being unpatentable over Kusonoki, (US 6,066,880) in view of Kiziyalli (US 5,767,557). Further, claims 23-26 were rejected under 35 USC 103(a) as being unpatentable over Ueno (US 5,998,828) in view of Kusonoki and Kizilyalli.

The Examiner rejected claims 1-9 and 22, indicating that Kusonoki at FIGS. 68-79; col. 3, lines 5-42; and col. 7, lines 60-65 disclosed all of the elements of claims 1-9 except the peak concentration positioned at a selected level below the gate dielectric, and asserted that this element could be found in Kiziyalli. Applicants respectfully disagree. Neither Kusonoki nor Kiziyalli disclose or suggest the placement of a buried channel configured to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer when the gate is biased with respect to the substrate. FIG. 75 in Kusonoki appears to be representative of the teaching that voltage threshold adjustment may be performed using a channel dope region which requires a p type region 3p such as is shown in FIGs. 76 and 77. This is an example of a conventional use of a buried channel having the same type dopants as the substrate for threshold adjustment purposes. In contrast, the functional limitation in claim 1, and as further recited in independent claims 2 and 3, requires the buried channel to be a different type than the substrate.

Claims 2-9 and 22 depend from claim 1 and are submitted to be allowable for at least the same reason. Moreover, as to claim 22, applicants submit that Kiziyalli

Kiziyalli relates generally to semiconductor PMOS devices having Indium or Gallium impurity concentrations for improved short channel characteristics (abstract). The Examiner indicated that Kiziyalli teaches forming a peak concentration of implanted dopants in the buried channel within a few hundred angstroms below the interface (see col. 5, lines 6-19). But even at this location, Kiziyalli fails to teach or suggest the peak concentration at a level selected to act as a supplemental gate dielectric layer.

Ueno relates generally to a semiconductor device achieving high voltage threshold values by different concentrations of nitrogen in the gate electrode

semiconductor device achieving high voltage threshold values by different concentrations of nitrogen in the gate electrode (abstract). Although the Examiner pointed to FIGs. 5-8 and col. 7, lines 19-30, Ueno teaches only a conventional buried channel for threshold voltage implant purposes at those locations. That is, the channel dope layer 104 is doped with the same type impurity as the substrate (well). See Tables 1-5. The channel described in Ueno as a channel doping layer is nothing more than a threshold adjust implantation. As noted, Ueno's channel is doped with the same type dopant as the underlying substrate. Thus Ueno fails to teach or suggest all elements of claim 23 since the p-type channel in a p-type substrate as indicated in Ueno (doped with boron), fails to teach or suggest causing the substrate portions above the selected level to act as a supplemental gate dielectric layer as required in the claim. Thus, for at least this reason, Ueno in combination with the other cited references fails to teach or suggest all elements of claim 23.

Claims 2-9, 22, and 24-26 are dependant claims, submitted to be allowable at least due to their dependencies form an allowable independent claim.

#### **Conclusion**

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. If any fees are due over and above the fees provided with the amendment, such fees may be charged to deposit account No. 12-2252 (client docket 01-721).

Respectfully submitted,  
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